A-Level Physics

Digital Signal Processing

Mark Scheme

Time available: 58 minutes
Marks available: 44 marks

Mark schemes

1. (a) $\bar{A}$ ✓

. B ✓

Ā **. B** ✓

Do not allow $\overline{\mathbf{A}+\overline{\mathbf{B}}}$

2

(b) EOR ✓

Accept: XOR ; EXOR; Exclusive OR gate

1

(c)

B	A	C	D	E	X	Y	Z
0	0	1	1	0	0	1	0
0	1	0	1	1	0	0	1
1	0	1	0	1	1	0	0
1	1	0	0	0	0	1	0

X and **Z** correct ✓

Y correct ✓

2

(d) NOR gate ✓

Also accept any of:

EXNOR; ENOR; XNOR; Exclusive NOR gate

1

(e)

X	Y	Z	
A = B	A < B	A > B	
A < B	A = B	A > B	✓
A < B	A > B	A = B	
A > B	A = B	A < B	

1

[7]

2. (a)
- When V_c reaches a value of V_u, the output voltage V_{out} drops LOW. ✓
- The capacitor now discharges through the resistor causing the value of V_c to fall. ✓
- When V_c reaches a value of V_L, the output voltage V_{out} jumps HIGH. ✓

3

(b) **Mark-to-space ratio**

R_B gets smaller and hence (t_H) is reduced

OR

R_A gets bigger and hence (t_L) is increased ✓

First mark: Either statement or equivalent labelled diagram(s).

Hence mark:space ratio is reduced / smaller ✓

Second mark: Conclusion

PRF = $\frac{1}{T} = \frac{1}{(t_H + t_L)} = \frac{1}{0.7C\ (2R+R_A+R_B)}$

The total resistance ($2R + R_A + R_B$) is constant ✓

As a result of a constant resistance in the circuit, PRF does not change ✓

First mark: explanation of how total resistance in the circuit affects the periodic time

Second mark: Conclusion.

4

[7]

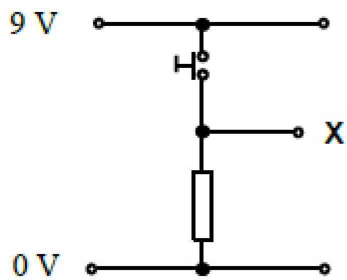
3. (a)

Inputs			Output
C	**B**	**A**	**Q**
0	0	0	0
0	0	1	0
0	1	0	0
0	1	1	0
1	0	0	1
1	0	1	0
1	1	0	1
1	1	1	1

*All Q **states** correct for 1 mark*

1

(b)



Correct orientation for resistor & switch ✓

*Correct tap-off point for **X*** ✓

2

(c)

$Q = \overline{(C.A) + (C.B)}$ Two correct brackets ✓

\+ with full bar ✓

Allow for 1 mark: $Q = \overline{C.(A + B)}$

2

(d) The gate acts as an inverter ✓

Accept 'NOT' as the function

1

(e) Must be a reason and a consequence for the mark. ✓

eg Uses only one type of logic gate so need to hold less stock

OR

Uses only one chip rather than two so circuit board can be smaller / less power needed / cheaper

Do not allow: Less complex circuit

1

[7]

4. (a) Difference: BCD counter outputs binary codes. A Johnson decade counter outputs a single output sequentially✓

Similarity: Both counters recycle at the 10^{th} pulse ✓

Both outputs described.

Condone – max counter value for 10^{th} pulse.

Accept: both counters count from 0–9

OR both counters count to 10

2

(b) Duty cycle:

From oscilloscope t_{on} = 3 div @ 50 µs / div = 150 µs
OR
t_{off} = 2 div @ 50 µs / div = 100 µs ✓

$$\frac{t_{on}}{(t_{on} + t_{off})} \times 100 = 60\% \quad \text{OR} \quad 0.6$$ ✓

(accept 'divisions' to signify the values of t_{on} and t_{off})

Frequency:

From CRO t_p = 5 div @ 50 µs / div
t_p = 250 µs

$f = 1/t_p$ = 4 kHz ✓

Only 1 mark for:

either of t_{on} or t_{off} correct but duty cycle wrong

OR

correct use of both wrong t_{on} and t_{off}

One mark for:

correct use of their $t_{on} + t_{off}$

3

(c) **BCD:** Q_2 = 600 / 10 = 60 Hz ✓

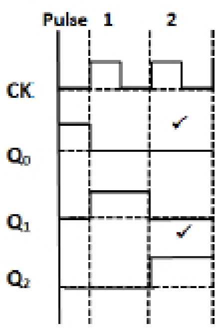
(only one pulse is produced in 10 clock pulses at Q_2)

Johnson: Q_2 = 600 / 10 = 60 Hz ✓

2

[7]

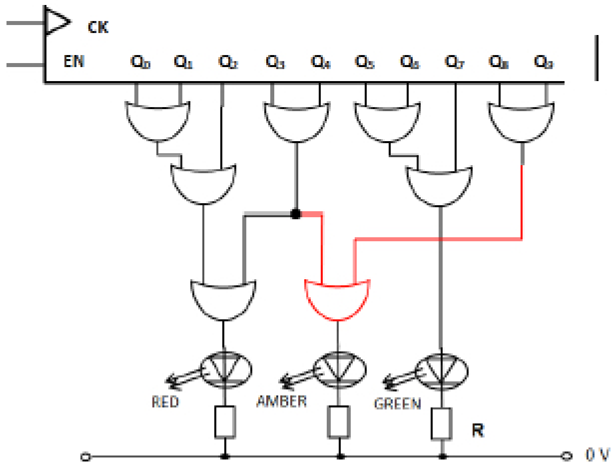
5. (a)



Flat line of Q_0 - 1 mark
Correct fall of Q_1 and rise of Q_2 - 1 mark

2

(b)



Logic OR gate correctly connected in position for 1 mark

1

(c) The ON time for the green LED is determined by:

the frequency of the clock ✓

the number of adjacent outputs that are OR'ed ✓

Accept reference to the period of the clock pulse.

2

(d) **R** = V_R / I ; **R** = (9 – 2.1) V ✓ / 9 mA

R = 6.9 V / 9 mA ; **R** = 767 Ω ✓

Minimum resistor value that can be used in order not to exceed 9 mA is 767 Ω.

The 720 Ω resistor range is (684 to 756) Ω and falls below this value so should not be used. ✓

OR

Calculation using 720 Ω ±5% Resistor range = (684 to 756) Ω ✓ leading to smallest current of 9.1 mA ✓

This current will exceed the permitted value of 9 mA. Don't use. ✓

$_1$One mark for voltage across the resistor

$_2$One mark for a suitable I-V-R calculation

$_3$One mark for conclusion with reason.

Use of error range to give max resistance must be seen in either $_2$ or $_3$ for that mark to be awarded.

3

[8]

6. (a)

A	B	a	b	c	d	e	f	g	Display
0	0	**0**	**0**	**0**	**1**	**1**	**1**	**0**	L
0	1	**1**	**0**	**1**	**1**	**0**	**1**	**1**	S
1	0	**1**	**0**	**1**	**1**	**0**	**1**	**1**	S
1	1	**0**	**1**	**1**	**0**	**1**	**1**	**1**	H

1 mark for row L

1 mark for row S (both)

1 mark for row H

3

(b) EXOR gate

1

(c) (i) Different combinations produce different brightness

1 Disadvantage

1

(ii) R=V/I; (5V − 2.2V) / 20mA; 2.8V / 20mA = 140Ω

1 mark for 2.8V drop

1 mark for answer

2

(iii) E24 = 150Ω

1 mark for answer

1

(8)