A-Level Physics

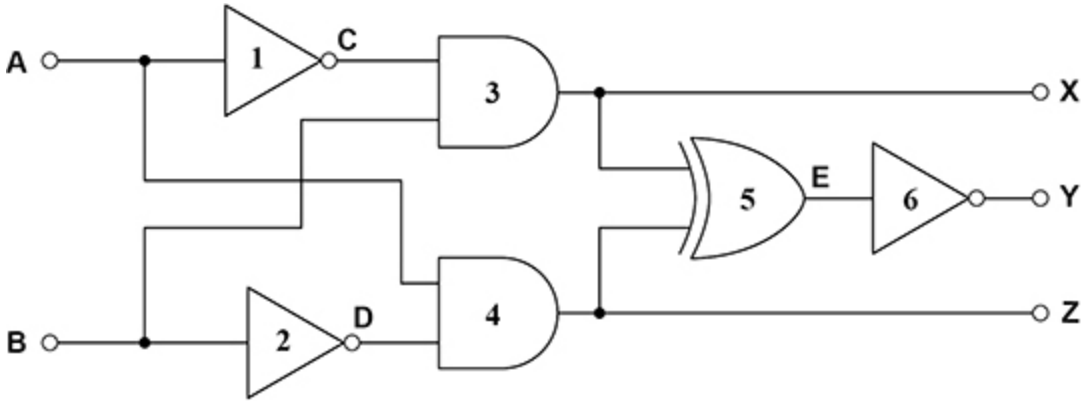
Digital Signal Processing

Question Paper

Time available: 58 minutes
Marks available: 44 marks

1. The diagram below shows a logic system made of logic gates labelled **1** to **6**

The logic system has inputs **A** and **B** and outputs **X**, **Y** and **Z**.



(a) Write the simplest Boolean algebra expression for output **X** in terms of inputs **A** and **B**.

X = _____

(2)

(b) State the name of logic gate **5** in the figure above.

_____

(1)

(c) Complete the table below, the truth table for this logic system.

B	A	C	D	E	X	Y	Z
0	0	1	1	0			
0	1	0	1	1			
1	0	1	0	1			
1	1	0	0	0			

(2)

(d) Suggest a single logic gate that can replace the combination of gates **5** and **6** in this system.

_____

(1)

(e) The logic system in above diagram is designed to indicate which of inputs **A** and **B** has the larger binary value, or whether the values are the same. Each decision is indicated by one of the outputs **X**, **Y** or **Z** becoming a logic 1

Which row identifies the outputs **X**, **Y** and **Z**?

Tick (✓) **one** box.

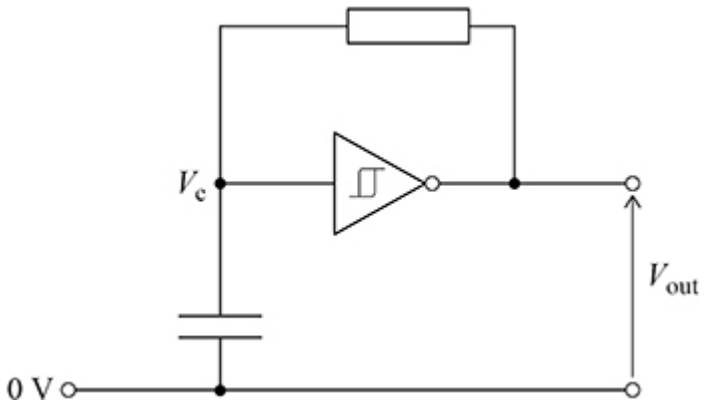
X	Y	Z	
A = B	A < B	A > B	
A < B	A = B	A > B	
A < B	A > B	A = B	
A > B	A = B	A < B	

(1)

(Total 7 marks)

2. **Figure 1** shows a type of NOT gate called a Schmitt Trigger. This is connected to a capacitor of capacitance C and a resistor of resistance R to make an oscillator circuit. The circuit is used to produce continuous clock pulses.

Figure 1



V_{out} switches HIGH or LOW when the input voltage V_c passes through one of two trigger voltage values.

The output voltage V_{out} switches to:

- LOW when V_c rises and reaches the upper trigger voltage V_U
- HIGH when V_c falls and reaches the lower trigger voltage V_L.

(a) Initially the capacitor is uncharged and V_c is at $0\ \text{V}$.

Explain the sequence of actions of this circuit as the output goes through one full cycle. The first two stages have been done for you.

You should refer to the RC circuit in **Figure 1** and to V_U and V_L in your answer.

Stage 1: Since V_c is LOW, the output is HIGH.

Stage 2: The capacitor now charges through the resistor, making V_c rise.

Stage 3: _____

_____

_____

Stage 4: _____

_____

_____

Stage 5: _____

_____

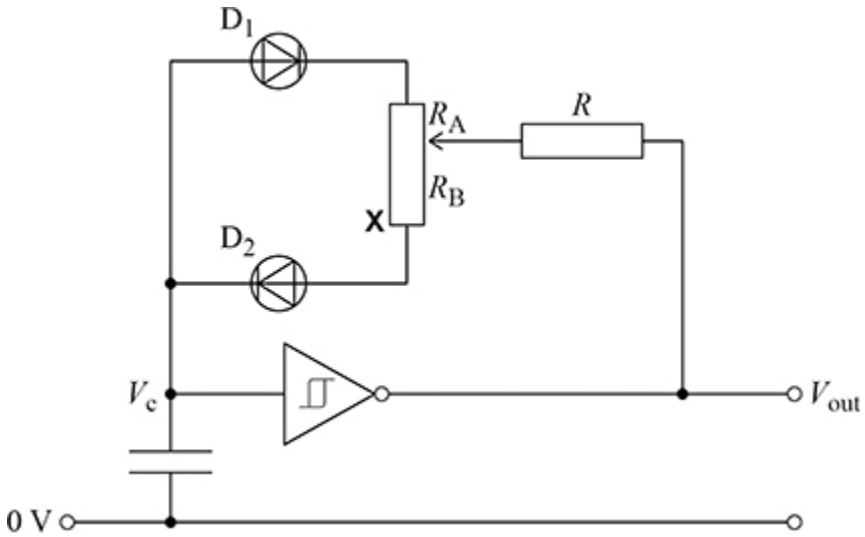
_____

(3)

(b) **Figure 2** shows the oscillator circuit after it has been modified by the addition of:

- two diodes D_1 and D_2
- a potential divider that has a total resistance value of (R_A + R_B).

Figure 2



In this particular circuit:

- the time t_H for the output signal to be HIGH is given by $t_H = 0.7C\ (R + R_B)$
- the time t_L for the output signal to be LOW is given by $t_L = 0.7C\ (R + R_A)$.

The slider of the potential divider is moved towards **X**, as shown in **Figure 2**.

State and explain the effect of this change on:

- the mark-to-space ratio (t_H : t_L)
- the pulse rate frequency (PRF).

mark-to-space ratio _____

_____

_____

_____

_____

_____

PRF _____

_____

_____

_____

_____

_____

(4)

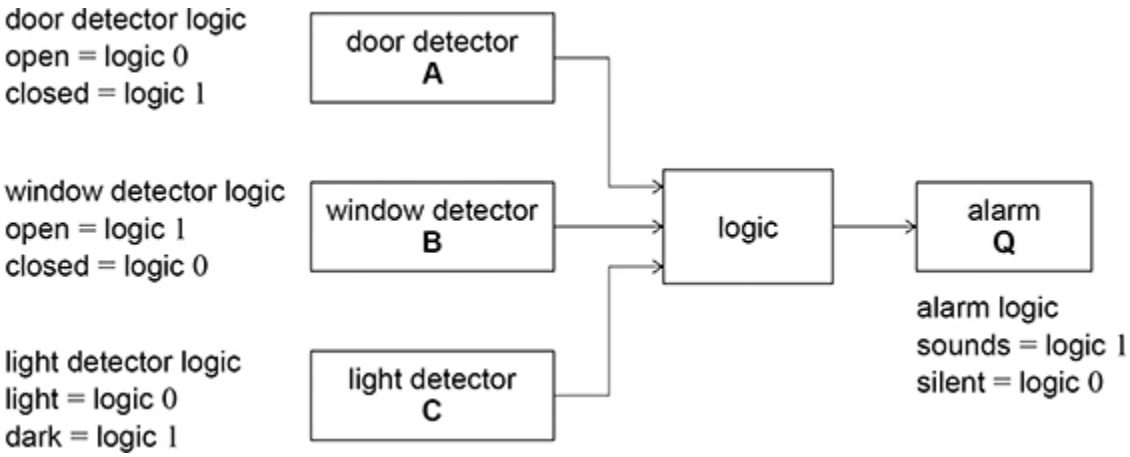
(Total 7 marks)

3. A burglar-alarm system in a house sounds an alarm during the hours of darkness when **one** of the following conditions is met:

- the door is opened
- the window is opened
- both the door and the window are opened.

Figure 1 shows the main burglar-alarm subsystems and the logic status for the inputs and output.

Figure 1



(a) The table below is a partially completed truth table for the logic subsystem.

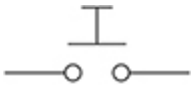
Inputs			Output
C	**B**	**A**	**Q**
0	0	0	0
0	0	1	0
0	1	0	0
0	1	1	0
1	0	0	1
1	0	1	
1	1	0	
1	1	1	

Complete the table above.

(1)

Figure 2 shows the symbol of the push-to-make switch used in the door detector. When the door is closed, the switch button is pushed down onto the contacts. It automatically releases when the door opens.

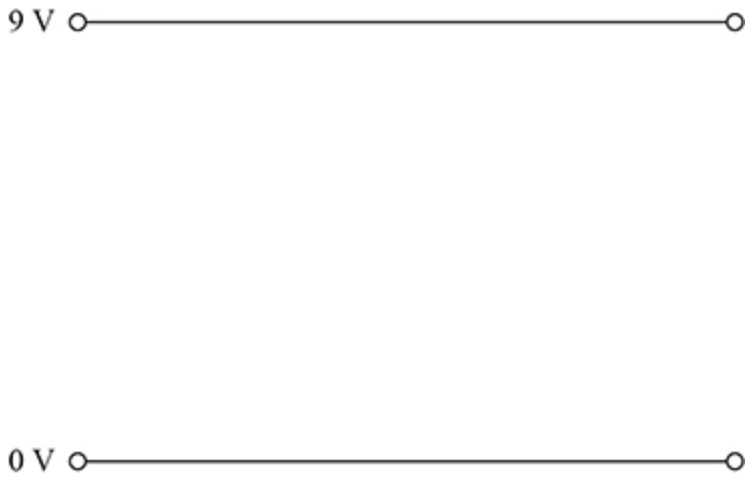
Figure 2



(b) Complete **Figure 3** to show how this switch, together with a 10 kΩ resistor, can be connected to create the door detector circuit in **Figure 1**.

Label the output of the circuit with an **X**.

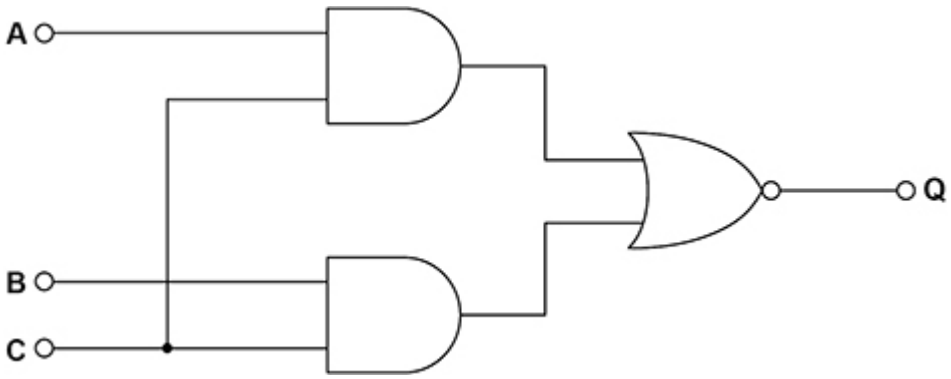
Figure 3



(2)

Figure 4 shows a logic circuit for a different alarm system.

Figure 4



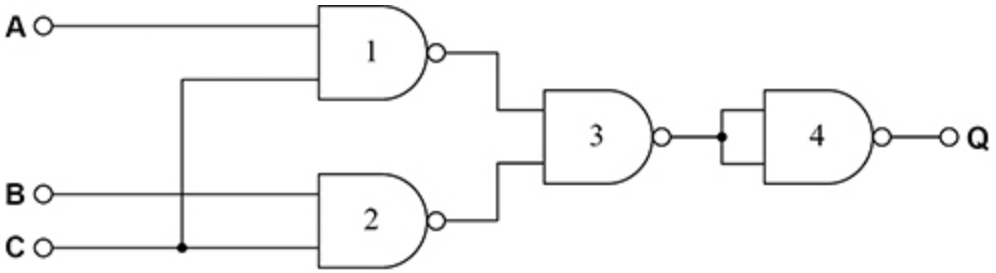
(c) Write the Boolean algebra expression for **Q** in terms of inputs **A**, **B** and **C**.
In your answer use only AND and NOR operators.

Q = _____

(2)

(d) **Figure 5** shows a logic circuit that has the same function as the circuit in **Figure 4**. Only one type of gate is used in the circuit in **Figure 5**.

Figure 5



State the logic function performed by gate 4.

_____

(1)

(e) Microchips containing two-input logic gates are mass-produced. Each microchip contains four identical logic gates.

A manufacturer of the logic circuit used in the burglar alarm chooses to make the circuit in **Figure 5** rather than that in **Figure 4**.

Suggest why.

_____

_____

(1)

(Total 7 marks)

4. A Johnson decade counter uses a Johnson counter together with decoding logic. This arrangement produces a single logic 1 at a series of outputs Q_0–Q_9 in a continuous sequence.

(a) Describe **one** functional difference and **one** functional similarity between how a Johnson decade counter and a BCD counter output their counts.

functional difference _____

_____

_____

_____

functional similarity _____

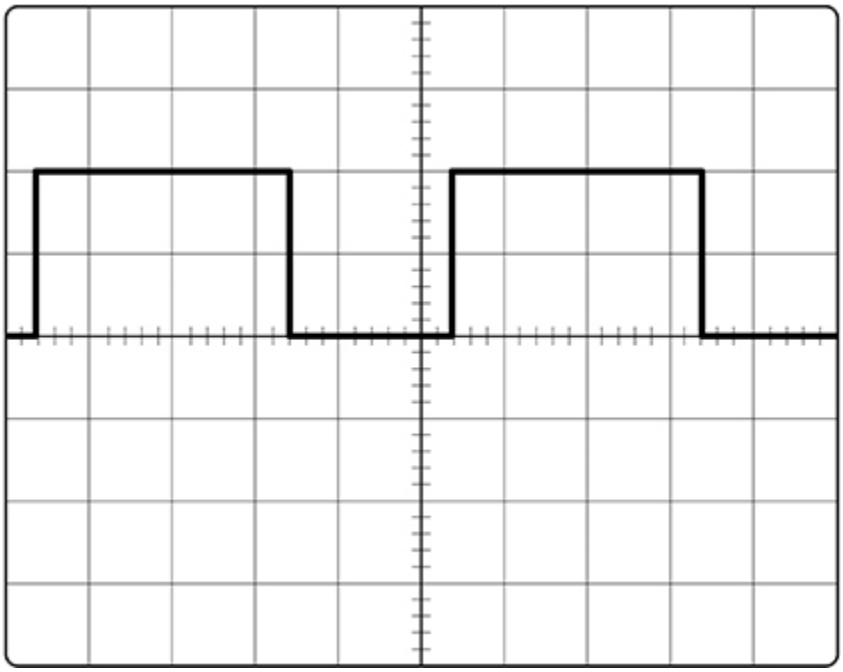
_____

_____

_____

(2)

(b) An astable oscillator produces a continuous train of pulses.
The figure below shows the display of the pulses on an oscilloscope.



The oscilloscope settings are:

voltage gain = 2 V / division
time-base = 50 μs / division.

Determine the duty cycle and frequency of the signal.

duty cycle = _____

frequency = _____ kHz

(3)

(c) The astable is adjusted to produce a 600 Hz test signal.

This signal is applied to the clock input of the BCD counter and to the clock input of the Johnson decade counter.

The outputs of the BCD counter are Q_0, Q_1, Q_2 and Q_3 where Q_0 is the least significant part of the output.
The outputs of the Johnson decade counter are Q_0, Q_1, Q_2 … Q_9.

Determine the frequency of the pulses available at Q_2 for each counter.

BCD counter: frequency of pulses = _____ Hz

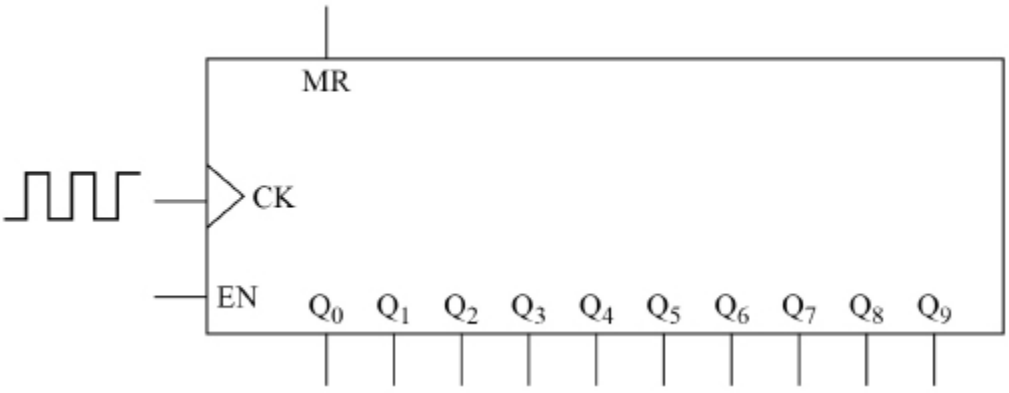
Johnson decade counter: frequency of pulses = _____ Hz

(2)

(Total 7 marks)

5. **Figure 1** shows the basic layout for a Johnson decade counter.
The main input is the clock (CK).
The main outputs are shown as Q_0 to Q_9.

Figure 1

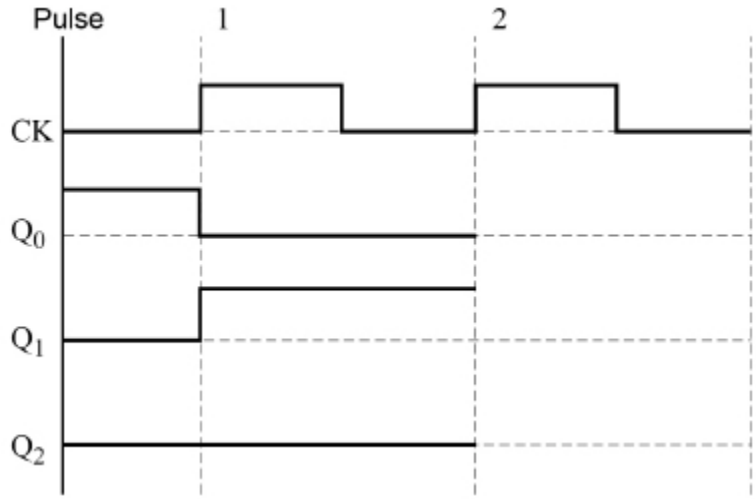


(a) **Figure 2** shows part of the timing diagram for a Johnson decade counter.

This timing diagram shows the output logic states against time. The counter is reset to make $Q_0 = 1$ and then the first two pulses are applied.

Complete **Figure 2** to show the logic states of Q_0, Q_1 and Q_2.

Figure 2



(2)

(b) A student sets up the counter to make the traffic light sequence:

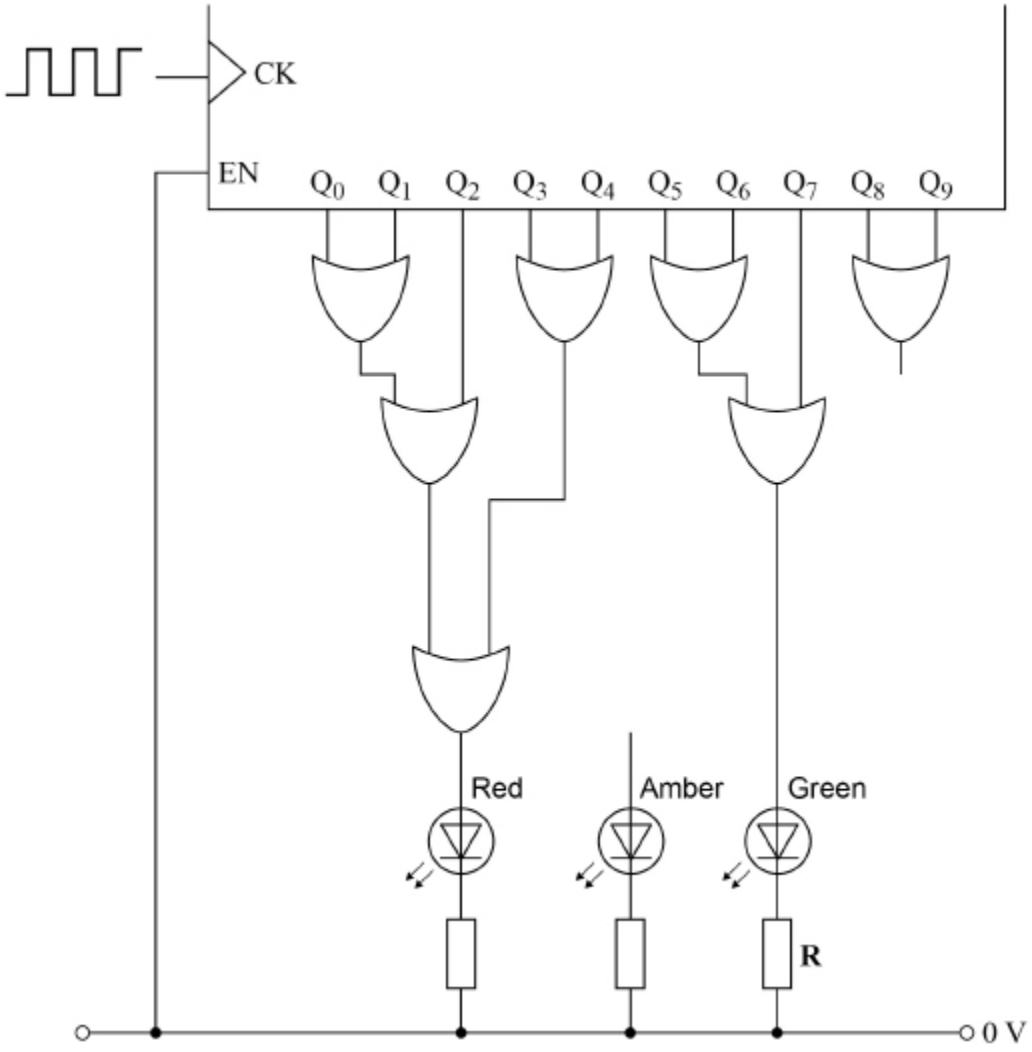
red → red + amber → green → amber

The sequence then repeats.

Figure 3 shows a partially completed diagram for producing this sequence.

Draw an OR gate and connections on **Figure 3** so that the LEDs go through the complete sequence.

Figure 3



(1)

(c) State **two** factors that determine the ON time for the green LED shown in **Figure 3**.

1 _____

_____

2 _____

_____

(2)

(d) The potential difference across the green LED is 2.1 V when it is lit. The current through it should not exceed 9 mA.

All logic gate outputs are:
logic low = 0 V
logic high = 9 V.

The student suggests that a resistor of resistance 720 Ω and a tolerance of ±5% should be used for **R**.

Deduce whether the student's suggestion would be suitable.

_____

_____

_____

_____

(3)

(Total 8 marks)

6. A fridge is fitted with a temperature-sensing unit to indicate whether the temperature inside the fridge is too high, too low, or at a safe temperature.
The system consists of a temperature sensor that produces a 2−bit binary output, a logic circuit and a low current, common cathode 7−segment display.
Figure 1 shows a block diagram of the system.

Figure 1

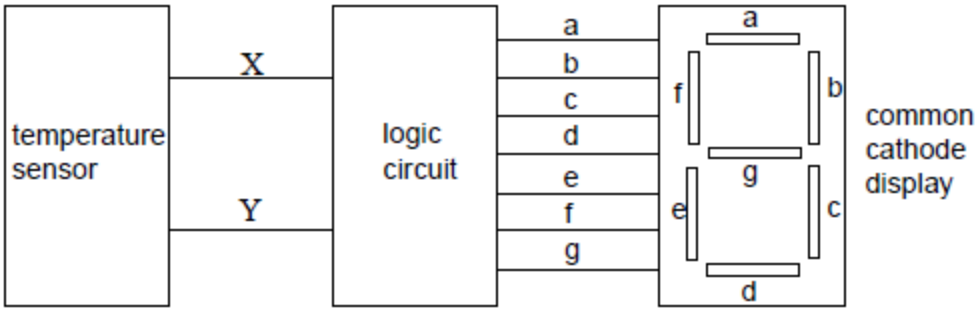


Table 1 shows the operation of the system.

Table 1

Fridge temperature	Temperature sensor output		7-segment display output
	X	Y	
< 3 °C	0	0	L
3 °C to 4 °C	0	1	S
4 °C to 5 °C	1	0	S
> 5 °C	1	1	H

Key
L = low
S = safe
H = high

(a) Complete **Table 2** to show the logic signals required on lines a to g to display the specified characters.

Table 2

X	Y	a	b	c	d	e	f	g	Display
0	0								L
0	1								S
1	0								S
1	1								H

(3)

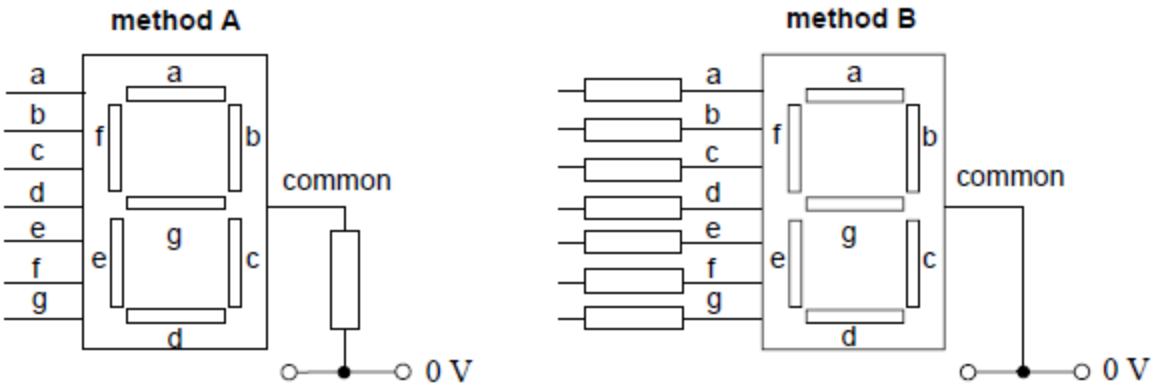
(b) Circle the single logic gate which would generate the required signal for segment **a**.

AND EXOR OR NAND NOR NOT

(1)

(c) The LEDs in the 7−segment display must be protected by current limiting resistors.
Figure 2 shows two methods, **A** and **B**, of connecting current limiting resistors.

Figure 2



(i) State **one** disadvantage of **method A**.

_____

_____

(1)

(ii) Calculate the value of the current limiting resistors required in **method B** to limit the current in each segment to 20 mA.
Assume the voltage from the logic circuit is 5 V and the forward voltage drop across each LED in the 7−segment display is 2.2 V.

_____

_____

_____

(2)

(iii) Circle the appropriate value for these resistors from the following list of E24 resistors.

110 Ω 150 Ω 270 Ω 1.1 kΩ 1.5 kΩ

(1)
(Total 8 marks)